

SPECIFICATIONS

INPUT

Data Inputs: 2 front-panel 34-pin connectors which accept complementary ECL signals; 100 Ω input impedance; 32 parallel bits can be accepted and stored in the memory word addressed at the strobe pulse arrival time; the memory address is automatically incremented by one at the end of the strobe pulse. The data must arrive within 5 nsec of the STrobe and remain valid for at least 25 nsec.

Write Strobe (STrobe): NIM: one Lemo-type front-panel connector with 50 Ω impedance; accepts a NIM level pulse with a minimum width of 10 nsec.

ECL: located on pins 33 and 34 of the upper 34-pin connector (DATA 0 - 15); the connector accepts a complementary ECL pulse with width of at least 10 nsec and 100 Ω input impedance. The leading edge of the strobe pulse must fall inside the data pulse and must arrive within 5 nsec; maximum frequency 15 MHz.

Clear (CLR): NIM: One front-panel lemo-type connector with 50 Ω impedance; accepts a NIM-level pulse with a pulse width of at least 10 nsec; resets the address counter.

OUTPUT

Acknowledge (ACK): NIM: front-panel Lemo-type connector, outputs NIM level pulses, minimum width 25 nsec. ECL: located on pins 33 and 34 of the lower 34-pin connector (DATA 16 - 31); the connector outputs a complementary ECL pulse with width of at least 25 nsec output suitable to drive 100 Ω lines.

Overflow (OV): NIM: front-panel Lemo-type connector, outputs NIM level pulses, minimum width 25 nsec.

GENERAL

Packaging: 6 U x 160 mm, single-width VME, in conformance with VME specification (ANSI/IEEE-1014C).

Operating Temperature: 10° to 50° C.

Storage Temperature: -30° to 85° C.

Maximum Humidity: 80% non-condensing at 30° C.

Power: +5 V at 1100 mA; -12 V at 500 mA.

TIMING

VME ACCESS time is measured as DS0/1 to DTACK. Table 1 shows typical times for various VME operations.

Data Transfer WRITE	<130 nsec
Data Transfer READ	<120 nsec
Block Transfer READ (1st word)	<120 nsec
Block Transfer READ	< 55 nsec
Read Address Counter	< 80 nsec
Set Mode Register	< 80 nsec

These times are conservative and assume that the Master asserts DS0/1 and AS simultaneously.

Table 1

FRONT-PANEL LEDS

VME Enabled Displays that the mode register is set to "FPP DISABLED" or that the jumper W2 is "on" and W1 is set "off".

VME Access Displays that an allowed access is being performed, and that the module is generating DTACK.

FP Enabled Displays that the mode register is set to FRONT PANEL ENABLED. Note that the FFP may be disabled because of an OVERFLOW.

FP Access Displays that a successful access via the Front Panel Port.

OVFL Displays that the memory address counter has exceeded the existing memory area.